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| 10/063,472 | 04/26/2002 | Hideharu Ozaki | 15483 | 1170 |

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| EXAMINER | |
|---|---|
| KERVEROS, JAMES C | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2133 | |

DATE MAILED: 10/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) |
|---|---|---|
| | 10/063,472 | OZAKI, HIDEHARU |
| | Examiner | Art Unit |
| | JAMES C KERVEROS | 2133 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *14 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) *5-20,25-29,31 and 33-36* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,21-24,30 and 32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 April 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. This Office Action is in response to AMENDMENT filed 6/14/2004, in reply to the Office Action mailed February 10, 2004.

### *Election/Restrictions*

2. Applicant's election without traverse of Fourth Species of FIG. 7, readable on claims 1-4, 21-24, 30 and 32 in Paper No. 4 is acknowledged.

Claims 5-20, 25-29, 31 and 33-36 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 4.

Claims 1-36 are still pending.

### *Drawings*

3. This application lacks formal drawings. The informal drawings filed in this application are acceptable for examination purposes. When the application is allowed, applicant will be required to submit new formal drawings.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Jaber et al. (US 5614838), ISSUED: March 25, 1997.

Regarding Claim 1, Jaber discloses an apparatus and method for high speed electronic components, for performing level sensitive scan design (LSSD) testing of the integrated circuit device under test (DUT), comprising:

A two-pulse generator (200, FIG. 2) and also described in (column 3, line 35-40), for generating a two pulse signal (CLKG 205) comprising a series of three pulses, FIG. 5, where the time duration of LSSDCCLK signal on line 403 controls the number of pulses being generated, (column 5, line 25-40) .The pulses are spaced apart from each other by a pulse interval such as (421 CLKC_INTERNAL) equal to a period of a test clock (211) which is input from an external source (203 OSC_IN), and supplying the generated two pulses (CLKG 205) to the scan path test circuit for performing a multiphase test of the high speed electronic component, device under test (DUT), FIG. 1.The external source (203 OSC_IN) is the source from which the output CLKG is generated. The test clock (211) is the free running version of global CLKG. Also, the clock signal CLKL is a relatively short duration pulse clock signal running at the same speed as global CLKG, which shows four pulses, where the two pulses are spaced apart by the same time interval as the COP_CLKG 211 period.

Regarding Claim 2, Jaber discloses a PLL circuit (204, FIG. 2) for multiplying a frequency of the external source (203 OSC_IN), which is proportional to the test clock (211) frequency for generating a test clock signal CLKG 205, also described in the

abstract, where a frequency multiplier circuit (204) for multiplying the test clock signal to a higher second frequency capable of operating the device under test.

Regarding Claims 3 and 4, Jaber discloses a gate signal generator for generating a gate signal to extract the test clock pulses comprising the STOPCLKG signal on line 207 and CLKGSTOPPED signal on line 209 to control the gating of the CLKG 205, including latch gate circuit for outputting the pulses, such as master latches (402, 406, 410, 414), and slave latches (404, 408, 412, 416), shown in FIG. 5.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 21-24, 30 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jaber et al. (US 5614838), ISSUED: March 25, 1997.

Regarding Claims 21-24, Jaber does not explicitly disclose a test board on which a semiconductor integrated circuit device is removably mounted and a clock generator mounted on the test board, for outputting a test clock. Jaber discloses a clock generator external source (203 OSC_IN), which is the input signal on line 203 to on-chip clock and phase lock loop circuit 204 for outputting a test clock (205) for testing a device under

test (DUT), FIGS. 1 and 2. However, it is well known in the art to removably mount an integrated circuit semiconductor device on a test board, such as on a PCB board. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use well known in the art, PCB mounting techniques, for the purpose of mounting a clock generator and an integrated circuit semiconductor device (DUT) on a PCB board, in the apparatus of Jaber, since the proximity of the clock generator source to the device (DUT) will result in the reduction of pick up noise and signal attenuation, thus maintaining the signal integrity of the high speed test clock.

Regarding Claims 30 and 32, Jaber does not explicitly disclose a frequency divider mounted on a test board. Jaber discloses a frequency divider (204) for dividing the frequency of the test clock (203) for measuring the frequency. However, it is well known in the art to mount a component such as frequency divider on a test board, such as on a PCB board. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use well known in the art, PCB mounting techniques, for the purpose of mounting a frequency divider on a PCB board, in the apparatus of Jaber, since the proximity of the frequency divider component to a measuring apparatus will result in the reduction of pick up noise and signal attenuation, thus maintaining the signal integrity of the high speed test clock.

### *Response to Arguments*

6. Applicant's arguments filed 6/14/2004 have been fully considered but they are not persuasive. Claims 21-24, 30 and 32 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Jaber et al. (US 5614838), and Claims 21-24, 30 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jaber et al. (US 5614838), as set forth in the present Office Action.

7. In response to applicant's argument, page 2, that Jaber does not disclose or suggest a two-pulse generator for generating a two pulse signal for scan path testing, according to the Office Action, above, Jaber discloses a pulse generator (200, FIG. 2) described in (column 3, line 35-40), for generating a series of gated pulses (CLKG 205) controlled by the time duration of the gate signal LSSDCCLK (403), which controls the number of pulses being generated, (column 5, line 25-40). Even though, FIG. 5 shows three pulses, it is clear that the pulse generator (200) is capable of generating two gated clock pulses only by controlling the time duration of gate signal LSSDCCLK (403).

Furthermore, the Applicant argues, page 3, that the CLKG 205, disclosed by Jaber, is a high speed system clock generated by an on- chip clock and phase lock loop circuit 204 and that the two-pulse signal of the present invention is generated by the test clock, which is not necessarily an on-chip clock. However, the above features, such as "high speed system clock generated by an on- chip clock", are part of the arguments only and are not part of the claims, and therefore do not carry patentable weigh. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In response to applicant's, page 4, argument that Jaber is nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's

endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, the Jaber reference is related to performing level sensitive scan design (LSSD) testing of the integrated circuit device under test (DUT) using a scan clock, which is supplied to the scan circuit.

In response to applicant's argument, page 4, with respect to Claims 21-24, 30 and 32 rejected under 35 U.S.C. 103(a) as being unpatentable over Jaber, that there is no suggestion to modify the Jaber reference, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the Examiner already admitted that Jaber does not explicitly disclose a test board on which an integrated circuit device is mounted. However, it is well known in the art to mount an integrated circuit device on a test board for testing purposes. Therefore, it would have been obvious to one of ordinary skill in the art to combine the teachings of Jaber with well-known test board techniques to arrive to Applicant's invention.

***Conclusion***

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C KERVEROS whose telephone number is (703) 305-1081. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

U.S. PATENT OFFICE
Examiner's Fax: (703) 746-4461
Email: james.kerveros@uspto.gov

Date: 12 October 2004
Office Action: Final Rejection

By: _____

JAMES C KERVEROS
Examiner
Art Unit 2133

GUY J. LAMARRE
PRIMARY EXAMINER